# Electronique d'EUSO-Phase A (Contribution au Red-Book d'Euso)

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**( Contribution au Red-Book d'EUSO)**

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# EUSO ELECTRONICS DESIGN DESCRIPTION

The EUSO electronics must ensure the operation and the control of the EUSO instrument so as to achieve the triggering and data taking of UHECR events. The first part of this section will present the principle of the EUSO detection system, expected signals and basic method of measurement. In a second part, the architecture and the components of the EUSO electronics will be described.

## 1 Principle of the EUSO Detection System

The EUSO detection system includes the EUSO telescope and the portion of the earth's atmosphere located in the field of view. EUSO operates as a time projection chamber to measure the properties of ultra high energy cosmic ray induced extensive air showers (EAS). A two dimension projection of an EAS is measured from the distribution of the light signals imaged in the segmented focal plane. The third projection, along the line of sight is measured from time delay differences. The absolute altitude of the EAS can be further evaluated from the reflected Cerenkov signal.

### 1.1. *Signals and backgrounds*

EUSO measures both the fluorescence photons and the Cerenkov photons generated by the EAS. Ionization of the nitrogen of the atmosphere by the charged particles in the shower leads to an isotropic emission of fluorescence light along the EAS trajectory. Fast charged particles emit Cerenkov light within a small cone along the shower direction. The Cerenkov light can be detected directly for EAS pointing to the telescope or by reflection from ground, sea or clouds for EAS pointing to the Earth.

An UHECR will appear as a luminous disc with a variable radius propagating almost at the speed of light along a segment of few to tens kilometers long. Its image will appear sequentially in the focal plane, starting with a faint signal and gradually increasing to a maximum before fading gradually away. The signal will depend on the energy, the altitude and the inclination of the shower. For a shower of $10^{20}$ eV, there will be typically few photoelectrons per pixel per microsecond on several aligned pixels during ~10-100 microseconds. This pattern will be in most cases followed with a time delay up to ~ 100 microseconds by the reflected Cerenkov light, peaked within one or two pixels and within a small time window of about a fraction of microsecond to few microseconds.

The EUSO electronics will have to distinguish this well defined space-time contiguity structure from the random background and other space-time correlated background signals of different origin (see the chapter on background). Measurements in micro satellite and balloon flights have determine the night time photon flux to be ~600 /m2/sr/ns. Accounting for absorption in the atmosphere and the instrument characteristics, the background expected at the detector level is ~0,5 photoelectrons (pe)/microsecond /pixel. In addition, some luminous phenomenon in the high atmosphere (airglow, blue jets ...) and human activities could produce a background few order of magnitude higher in some localized area.

### *1.2. Principle of measurement and triggering*

The basic method of measurement and triggering exploits the single photon counting technique. A charge integration approach is also implemented to handle signals at high energy and from strongly reflected Cerenkov light. With both analogue and digital electronics, the

detection is possible with a threshold as low as a fraction of the mean amplitude of the single photoelectron up to about 4000 photoelectrons, covering a dynamical range of 4 orders of magnitude.
As shown in a previous section, MAPMTs are physically grouped into Microcells of 4 PMT each. Several (~ 9) Microcells form a PhotoDetector Module (PDM). The triggering logic is based on almost independent modules called Macrocells, each with its own electronics. Practically, a Macrocell will correspond to a PDM of 36 MAPMT of 36 pixels each. Rows wire-or'd and columns wire-or'd routing connections have been adopted inside every single Macrocell. Each pixel can be identified by its position in X or Y in the Macrocell, diminishing the number of information that needs to be read-out. A "free running" method has been adopted to store temporarily the information in cyclic memories and recuperate the relevant data at the time that a good trigger signal occurs.

To eliminate background events, the EUSO system electronics operates with several trigger levels.

a) Each time the analogue threshold is exceeded, a fast discriminator recognizes the arrival of a single photoelectron event. The pulse is counted by a pixel-level counter.
b) When the pre-set counter value (PIXEL_THR) is reached within a given GTU(Gate Time Unit), a pixel-level trigger is issued, the X,Y lines of the pixel are marked into the X,Y memory, the pulse counting output is enabled during the remaining GTU time.
c) If the preset counter value (MACROCELL_THR) at the Macrocell level is reached within a given GTU, due to the pulses coming from the ENABLE-ed pixels, a Macrocell-level trigger is then issued.
A hard wired XY proximity device for adjacent GTU's at the Macrocell level is under study to further reject fake events in presence of large photon background.
d) The software reconfigurable System Trigger will continuously monitor the Macrocell-level trigger activity searching for patterns. When the given software criteria for a valuable pattern are met, the System Trigger will issue a system–level trigger and start the readout sequence after a preset exposure time.

Three trigger modes are considered in the present base line:
- Normal mode with a GTU of 2.5 microseconds for routine data taking
- Calibration mode with a GTU of few hundred nanoseconds, for calibration runs with dedicated light sources.
- Slow mode with a programmable GTU up to 1ms, for the study of meteorites and other atmospheric luminous phenomenon.

An auto-level-trigger function within the system trigger is also under consideration. This would allow the instrument to be set at the optimum trigger levels in case of varying background conditions due to slowly transient phenomena (moon phase, clouds coverage, large urbanized area and so on).

## 2. Architecture of EUSO Electronics

The EUSO Electronics can be divided into the following two main parts:
Focal Surface Electronics (subsubsystem of the FS subsystem): including all the electronics needed to bias and read out the 5544 MAPMTs up to the front end and Macrocell-level trigger. All this electronics is conceived as being physically part of the Focal Surface Assembly
Control Electronics (subsubsystem of the system electronics subsystem): including all the electronics needed for the instrument operation. All this electronics is conceived as being assembled into a standard electronics box named TCU (Trigger and Control Unit).

## 2.1. FOCAL SURFACE ELECTRONICS

The Focal Surface electronics includes the following items: the Front End Electronics (ASIC), the ReadOut & Control (RO&C) Electronics, HV Voltage dividers for the MAPMTs and Focal Surface Power Supply Subsystem.

### Front End Electronics

The EUSO Front End Electronics will be implemented in the form of an Application Specific Integrated Circuit (ASICs).The EUSO ASIC will provide both the MAPMT signal I/F and the pixel-level trigger. A simplified block-diagram of the baseline ASIC implementation referring to a 36 anodes MAPMT, is shown in Fig. 2.1.

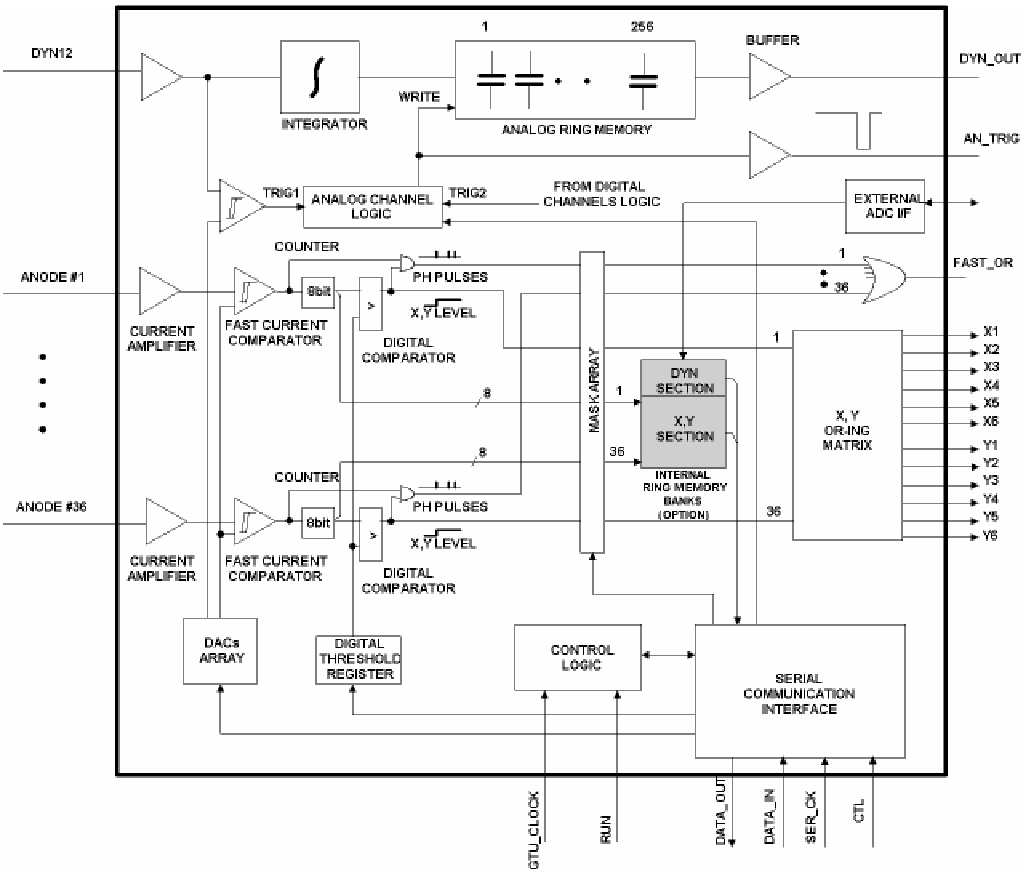


Fig. 2.1 EUSO ASIC baseline block diagram

The main functions of the EUSO ASIC are the following:

a) Collect the anodic signals via DC coupling;
b) Discriminate the amplified anodic signals above a programmable analogue threshold;
c) Provide a photon counting capability with less than 10 ns double-hit resolution;
d) Compare for every pixel the counted events within a given integration time with a programmable digital value (PIXEL_THR);
e) Enable the next incoming pulses from that channel to be routed out along a fast digital channel (FAST_OR) and activate the associated “X” and “Y” address lines ;
f) Integrate dynode signals and store in analogue memories;
g) Accept commands, parameters and settings from a serial line and Read out through a serial line.

To better fulfill the science requirements, and as possible options presently under study, the ASIC will also include a set of built-in ring memories (128GTU depth), a “time stamp” circuitry and a set of “anode” analogue channels working with a principle similar to the dynode one. They will be included if compatible within the power and mass budgets and after successful prototype testing.

**RO&C Functional and architectural description**

The preliminary architectural block diagram of the Read-out & Control Board is sketched in Fig. 2.1.

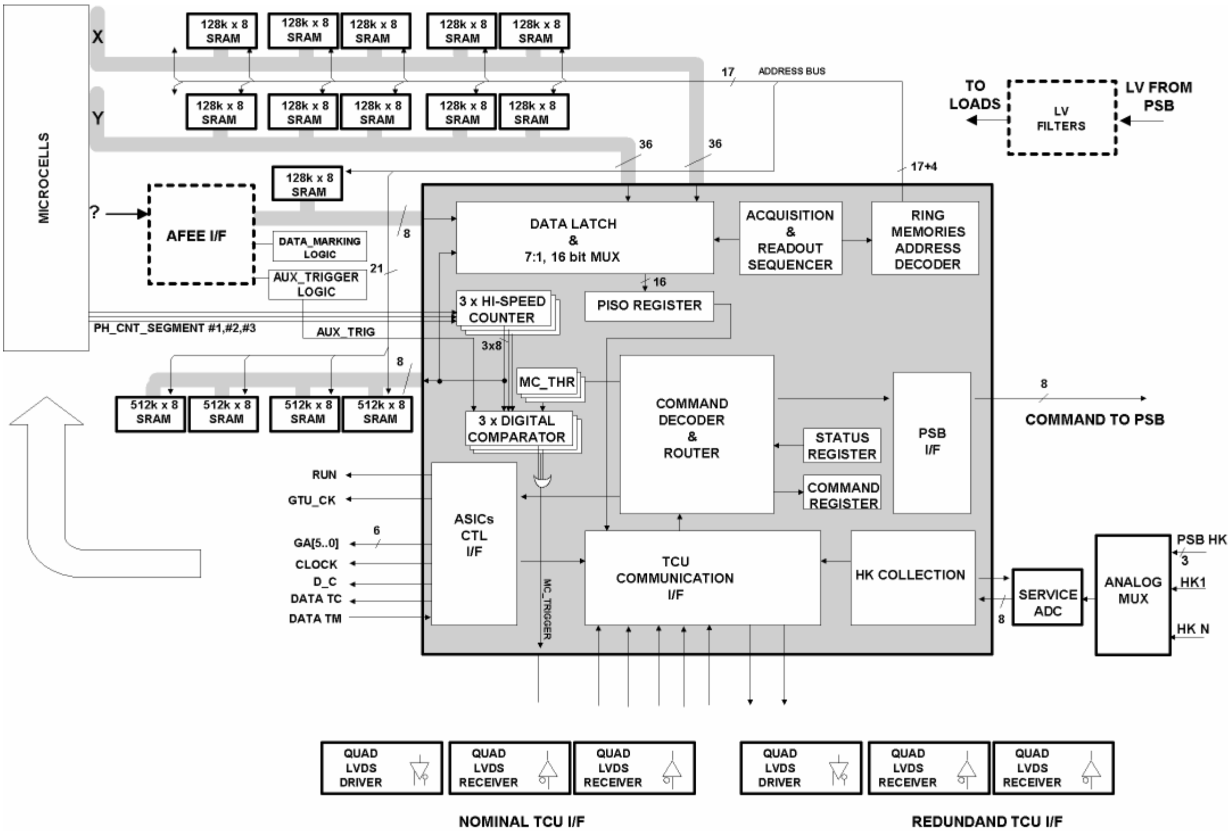


Fig. 2.2. Preliminary architectural block diagram of the Read-out & Control Board. The shown example is for a 9 Microcell PDM.

The basic structure of the RO&C electronics contains:

a) The Microcell Array I/F, mainly the X, Y and PH_CNT ring memories and AFEE ring memories, some strobe lines and the communication bus;
b) The AFEE I/F;
c) The Power Supply System I/F, mainly the power lines and some command/HK lines;
d) The TCU I/F, mainly the proper set of serial-parallel converters and driver/receivers;
e) Three 8-bit counter (one for each trigger segment) and a digital threshold register used to generate the MC_TRIGGER signal;
f) Digital multiplexers connected to a parallel-serial register used during data download;
g) Command Decoder & Router logic;
h) A service ADC (with an analogue multiplexer) used to collect the PDM data (e.g. voltages, temperatures...).

In the present baseline, all the interfaces between Macrocells and TCU are digital balanced differential lines based on a RS422-like model (possibly implemented as LVDS). An option under study is to implement an optical (IR) link between the PDMs and the TCU to reduce the harness mass. The System Trigger logic is mainly implemented within an FPGA to allow flexibility. The FPGA itself has to be SW-reconfigurable by proper writing of its configuration registers.

Most of the Read Out and Control blocks will be implemented into a dedicated FPGA hereafter named "Control Logic FPGA".
The **Control Logic FPGA** will have the following functions:

a) Generate the ASIC setting parameters;
b) Generate the GTU_CLOCK signal to reset the internal counters of all ASIC's and Macrocell's at the beginning of each GTU time window; and to load, the X and Y lines & PH_CNT counters into Macrocell ring memories at the end of each GTU window;
c) Manage the writing of the memories and the address generation for the "ring memory" operation;
d) Receive from the TCU the SAVE_FRAME signal;
e) Manage the reading of the memories and the address generation during data download;
f) Drive the multiplexer address lines when the data are streamed from the memories into a parallel-in-serial-out register;
g) Sent Telemetry Data to the TCU by means of the serial interface.

**HV Voltage dividers for the MAPMTs**
The baseline MAPMT sensors (Hamamatsu 7600 / R8900 series) are 12-dynode MAPMT. In the present baseline, each MAPMT has its own Voltage Divider (VD) which is implemented on the micro-cell base-board PCB.

## *Trigger and Control Unit (TCU)*

The EUSO instrument baseline includes a Nominal and a (cold) Redundant Trigger and Control Unit (TCU) which is the electronics box providing the I/F with the CEPF.
The TCU will be an intelligent unit including a proper microprocessor with dedicated SW running on it both for Common Services and for Science Data Processing.
The definition status of this section of the EUSO Electronics could be detailed only after the other part of the instrument will be thoroughly defined.
A survey of all its envisaged functions is given in the following.
The Trigger & Control Unit performs the following functions:

a) System Trigger;
b) Focal Surface Interface;
c) Trigger and Control Handling;
d) Collection and preprocessing of the scientific and HK ( House Keeping) data;
e) Preparation, storage and transmission of the Scientific and HK Telemetry packets;
f) Management of the power distribution and the configuration to the PDM's;
g) Management of the lid mechanism (motor drivers and position sensors), of the Thermal Control System (heaters drivers and sensors)and Atmospheric Sounding Subsystem I/F (LIDAR) ;
h) Management of emergency situations.

These functions are described with more details in the document EUSO_EL_SP-001.

**Addentum: Handling of very intense light signals**

In the base line design, the EUSO Frond End Electronics will be able to cover 4 order of magnitude using both single counting technique with a threshold of a fraction of photo electron and charge integration method to handle signals up to few hundred photoelectrons per GTU per pixel and few thousand photoelectrons within 1 GTU (2,5μs) per PMT.

However, lightning, meteorites or other unexpected atmospheric or man made phenomena may produce light signals exceeding this value. In this case, the integrator will be saturated; no signal will be delivered after a first trigger indicating the crossing of the higher level threshold of the dynode signal.

Adaptations are proposed to maintain the front End electronics active and to collect data while such phenomena occur. The principle is the following: each time the higher dynode level threshold is attained; the content of a dedicated counter is incremented, and the integrator is reset to zero for about 100ns. The dynode channel is then active again and will be ready to collect other incoming photoelectrons. The number of counts within one GTU will provide information on the intensity of the flux.

With this implementation, the EUSO Front End electronics is expected not to be blinded by very intense light signals. The largest possible input signals will be limited however by the characteristics of the MAPMT and the voltage divider design.

The information (i.e. number of excursion over ~2000pe) obtained within a time window less then 1 GTU (2,5μs) may be used for PMT protection against accidental exposure to strong light. An alert signal may be send to the TEO which could make the decision to turn down or not in part or in total the high voltage.

**Documentations**

- Analog Front End Electronics Phase A Specification and Design EUSO-AFEE-SP-001-1
- DFEE Phase A Specification and Design document EUSO-DFEE-SP-001-1.1
- EUSO-FEE-SP-001-1.
- Read-out, trigger and Data Handling Approach for the EUSO experiment, EUSO-TEO-REP-001-1